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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,157	12/30/2003	Carlos J. Gonzalez	SNDK.348US0	7914

66785 7590 02/21/2008

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
02/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,157	GONZALEZ ET AL.	
	Examiner	Art Unit	
	ZHUO H. LI	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/24/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action has been modified in respond to the Amendment filed on 1/24/2008. Accordingly, claims 1, 35 and 37-42 are canceled, and claims 2-17 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 2-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (US 2002/0099904) in view of Chien et al. (US PAT. 6,742,078 hereinafter Chien).

Regarding claim 4, Conley discloses a memory system (figure 2) including a controller (301, figure 2) and a non-volatile memory, i.e., flash memory (figure 2), wherein the non-volatile memory is comprises of a plurality of units of erases (85-88, figure 15), wherein the controller access the non-volatile memory according to a set of metablock links ([0066]), each comprised of a plurality of units of erase, wherein the controller establishes the set of metablock linkings in a deterministic manner ([0067]). Conley differs from the claimed invention in not specifically teaching the steps of storing a record of the metablock linkings is stored in the non-volatile memory, determining that a unit of erase in a first of said metablock linkings is defective, updating the first metablock linking so that it no longer contains said defective unit of erase, and storing a record of the updated linking in the non-volatile memory. However, Chien discloses a flash memory system comprising four different types of blocks, data blocks, spare blocks, a new block and a link-table blocks (col. 2 lines 35-53), wherein the link-table blocks comprising a link table which it is used to record the link relationship between the logic block and the actual block (col. 3 lines 51-57 and col. 4 line 55 through col. 5 line 3). In addition, Chien further discloses the method comprising determining that a unit of erase in a first of the metablock linkings is defective (col. 3 lines 43-46), updating the first metablock linking so that it no longer contains the defective unit of erase, i.e., stored updated data in a substituted block (col. 3 line 63 through col. 4 line 20), and storing a record of the updated linking in the non-volatile memory (col. 4 lines 10-20). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Conley in having the steps of storing a record of the metablock linkings is stored in the non-volatile memory, determining that a unit of erase in a first of said metablock linkings is defective, updating the first metablock linking so that it no longer

contains said defective unit of erase, and storing a record of the updated linking in the non-volatile memory, as per teaching of Chien, because it provides protection against power failure to protect the data link structure and improves stability (see Chien, col. 1 lines 12-15).

Regarding claim 2, Conley discloses the record is a completed specification of the set of linkings in terms of units of erase ([0068]).

Regarding claim 3, Conley discloses the set of linkings is formed according to a rule and the record consists of those linkings that are exceptions to the rule ([0066]).

Regarding claim 5, Chien discloses the method wherein the updating comprises replacing the defective unit of erase with another one of the units of erase, i.e., use a substituted block to stored updated data to replace the defective or original block (col. 3 line 43 through col. 4 line 20).

Regarding claim 6, Chien discloses the method wherein another one of said unit of erase is selected from a list of unlinked units of erase, i.e., spare blocks (col. 3 line 63 through col. 4 line 3).

Regarding claim 7, Chien discloses the method wherein the list of unlinked units of erase is maintained in the non-volatile memory (figure 1 and col. 3 lines 8-30).

Regarding claim 8, Chien discloses the method further comprising subsequent to the replacing the defective unit of erase with another one of the units of erase, i.e., use head and tail pointers to pick the next available spare block in the spare block stack as a substitute block (col. 3 lines 22-41), updating the list of unlinked units of erase (col. 5 lines 18-45).

Regarding claim 9, Chien discloses the method wherein another one of the units of erase is selected from a unit of erase formerly belonging to another linking (col. 4 lines 4-20).

Regarding claim 10, Conley discloses a memory system (figure 2) including a controller (301, figure 2) and a non-volatile memory, i.e., flash memory (figure 2), wherein the non-volatile memory is comprises of a plurality of units of erases (85-88, figure 15), wherein the controller access the non-volatile memory according to a set of metablock links ([0066]), each comprised of a plurality of units of erase, wherein the controller establishes the set of metablock linkings in a deterministic manner ([0067]). Conley differs from the claimed invention in not specifically teaching the steps of storing a record of the metablock linkings is stored in the non-volatile memory, maintaining a list of unlinked units of erase, determining that one or more units of erase in a first of said metablock linkings is defective, and adding the non-defective units of erase in the first metablock to the list of unlinked units of erase. However, Chien discloses a flash memory system comprising four different types of blocks, data blocks, spare blocks, a new block and a link-table blocks (col. 2 lines 35-53), wherein the link-table blocks comprising a link table which it is used to record the link relationship between the logic block and the actual block (col. 3 lines 51-57 and col. 4 line 55 through col. 5 line 3). In addition, Chien further discloses the method comprising maintaining a list, i.e., spare block stack (figure 4), of unlinked units of erase, determining that one or more units of erase in a first of the metablock linkings is defective, and adding the non-defective units of erase in the first metablock to the list of unlinked units of erase (col. 3 line 65 through col. 4 line 20 and col. 5 lines 18-30). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Conley in having the steps of storing a record of the metablock linkings is stored in the non-volatile memory, maintaining a list of unlinked units of erase, determining that one or more units of erase in a first of said metablock linkings is defective, and adding the non-defective units of

erase in the first metablock to the list of unlinked units of erase, as per teaching of Chien, because it provides protection against power failure to protect the data link structure and improves stability (see Chien, col. 1 lines 12-15).

Regarding claim 11, Conley discloses a memory system (figure 2) including a controller (301, figure 2) and a non-volatile memory, i.e., flash memory (figure 2), wherein the non-volatile memory is comprises of a plurality of units of erases (85-88, figure 15), wherein the controller access the non-volatile memory according to a set of metablock links ([0066]), each comprised of a plurality of units of erase, wherein the controller establishes the set of metablock linkings in a deterministic manner ([0067]). Conley differs from the claimed invention in not specifically teaching the steps of storing a record of the metablock linkings is stored in the non-volatile memory, determining that a unit of erase in a first of said metablock linkings is defective, determining whether an alternate unit of erase is available for the defective unit of erase, and in response to determining that an alternate unit of erase is not available, removing the first metablock from the set of metablock linkings. However, Chien discloses a flash memory system comprising four different types of blocks, data blocks, spare blocks, a new block and a link-table blocks (col. 2 lines 35-53), wherein the link-table blocks comprising a link table which it is used to record the link relationship between the logic block and the actual block (col. 3 lines 51-57 and col. 4 line 55 through col. 5 line 3). In addition, Chien further discloses the method comprising determining that a unit of erase in a first of the metablock linkings is defective, determining whether an alternate unit of erase is available for the defective unit of erase (col. 3 line 65 through col. 4 line 3), in response to determining that an alternate unit of erase is not available, removing the first metablock from the set of metablock linkings (col. 3 lines 43-46).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Conley in having the steps of storing a record of the metablock linkings is stored in the non-volatile memory, determining that a unit of erase in a first of said metablock linkings is defective, determining whether an alternate unit of erase is available for the defective unit of erase, and in response to determining that an alternate unit of erase is not available, removing the first metablock from the set of metablock linkings, as per teaching of Chien, because it provides protection against power failure to protect the data link structure and improves stability (see Chien, col. 1 lines 12-15).

Regarding claim 12, Conley discloses the non-volatile memory comprises a plurality of quasi-independent arrays (figure 2), and each of the plurality of units of erase in a given one of the metablock linkings are from a different one of the quasi-independent arrays (figures 15-16 and [0068]).

Regarding claim 13, Conley discloses the non-volatile memory comprises a plurality of quasi-independent arrays (figure 2), and the plurality of units of erase (figure 8) in a given one of the metablock linkings ([0054]), the metablock linkings are comprised of pairs of units of erase from the same quasi-independent array (figure 15), wherein each of the pairs are from a different one of said quasi-independent arrays (figure 16 and [0068]).

Regarding claim 14, Chien discloses a quasi-independent arrays, i.e., flash memories (FM0 – FM3, figure 7) are on separate chips (item a-d, figure 7 and col. 5 lines 31-45).

Regarding claim 15, Chien discloses the method wherein the record of the metablock linkings is stored in a portion of the non-volatile memory other than those assigned for user data (col. 4 line 35 through col. 5 line).

Regarding claim 16, Conley discloses each of the units of erase is comprises of plurality of sectors (80-83, figure 15), and each of the sectors includes a data area (85, figure 15), and an overhead area (50, figure 10), and wherein the record information for those units of erase containing data is maintained in their overhead area ([0055]).

Regarding claim 17, Chien discloses the method wherein the record information for those units of erase without data is maintained in a portion of the non-volatile memory other than those assigned for user data, i.e., spare block stack (figure 4).

Response to Arguments

4. Applicant's arguments filed 1/24/2008 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., linking of multiple physical blocks in the composite metablock structure) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In the case, all the claimed limitations as recited in claim 4 are rejected by the combination of Conley and Chien. It is noted that Conley clearly discloses a

memory system (figure 2) including a controller (301, figure 2) and a non-volatile memory, i.e., flash memory (figure 2), wherein the non-volatile memory is comprises of a plurality of units of erases (85-88, figure 15), wherein the controller access the non-volatile memory according to a set of metablock links ([0066]), each comprised of a plurality of units of erase, wherein the controller establishes the set of metablock linkings in a deterministic manner ([0067]). The utilize of Chien is for teaching the concept of storing a record of the link relationship between the logic block and the actual block (col. 3 lines 51-57 and col. 4 line 55 through col. 5 line 3), determining that a unit of erase in a first of the block linkings is defective (col. 3 lines 43-46), updating the first block linking so that it no longer contains the defective unit of erase, i.e., stored updated data in a substituted block (col. 3 line 63 through col. 4 line 20), and storing a record of the updated linking in the non-volatile memory (col. 4 lines 10-20) as recited in claim 4, thereby providing protection against power failure to protect the data link structure and improving stability (see Chien, col. 1 lines 12-15). Therefore, for at least these reasons, it is respectfully submitted that a rejection of claim 4 under U.S.C. § 103(a) as being unpatentable over Conley in view of Chien is well founded and that claim 4, along with its dependent claims (claims 2, 3, 5-9, and 12-17), are rejected.

In response to applicant's argument for claims 10 and 11 that Chien fail to show the use of metablocks, it is noted that Conley clearly discloses a memory system (figure 2) including a controller (301, figure 2) and a non-volatile memory, i.e., flash memory (figure 2), wherein the non-volatile memory is comprises of a plurality of units of erases (85-88, figure 15), wherein the controller access the non-volatile memory according to a set of metablock links ([0066]), each comprised of a plurality of units of erase, wherein the controller establishes the set of metablock

linkings in a deterministic manner ([0067]). The utilize of Chien is for teaching the concept of storing a record of the link relationship between the logic block and the actual block (col. 3 lines 51-57 and col. 4 line 55 through col. 5 line 3), as well as the remaining claimed elements as recited in claims 10-11. Note the claimed limitations are rejected by the combination of Conley and Chien and the motivation is to provides protection against power failure to protect the data link structure and improves stability (see Chien, col. 1 lines 12-15). Therefore, for at least these reasons, it is respectfully submitted that a rejection of claims 10 and 11 under U.S.C. § 103(a) as being unpatentable over Conley in view of Chien is well founded.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Mon - Fri 10:00am - 6:30pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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